Remarks

Applicant has filed a Request for Continued Examination together with this Amendment is in response to the final Office Action dated September 26, 2003. Claims 1, 3-4, 8, 23, 24, 27 and 38-39 have been amended. Claims 9-22 have been canceled without prejudice. Claims 1-8 and 23-39 are currently pending. Reexamination and reconsideration are respectfully requested.

Claims 1-3 and 7-8 were rejected under 35 U.S.C. 102(b) as unpatentable over U.S. Patent No. 6,300,670 to Kramer et al (hereinafter "Kramer"). The rejection is respectfully traversed.

Applicant respectfully submits that the Examiner cited no portion of the art that describes or suggests a method including " a multi-layer electrode . . . formed to include a first conducting layer and a second conducting layer formed in direct contact with the first conducting layer, wherein the first conducting layer is positioned between the second conducting layer and the first surface of the semiconductor chip, and then digging a hole from a second surface of the semiconductor chip until the electrode is exposed" as recited in claim 1, as amended.

The Examiner cited col. 4, lines 11-15 for the statement that "layer 130 includes a plurality of metallization layers." Office Action at page 2. However, applicant notes that Kramer states at col. 4, lines 11-15, that ". . .layer 130 may actually comprise several layers of metallization and intervening insulating material." Thus Kramer describes the use of an intervening insulating layer between metal layers. Accordingly, applicant respectfully submits that the Examiner's citation to Kramer does not describe or suggest the multi-layer electrode with first and second conducting layers formed "in direct contact" as recited in claim 1. As a result, for at least the above reason, the rejection of claim 1 and its dependent claims 2-3 and 7-8 should be withdrawn.

Claims 4-6, 24-26 and 32 were rejected under 35 U.S.C. 103(a) as unpatentable over U.S. Patent No. 6,114,221 to Tonti et al. (hereinafter "Tonti") in view of Kramer. The rejection is respectfully traversed.

Independent claim 4 recites a method including "forming a dielectric layer on the second surface of the first semiconductor chip and on the first semiconductor chip in the hole, wherein the dielectric layer has an opening and the electrode is exposed through the opening". Claim 24

recites a method including "forming a dielectric layer on the interior sidewalls of the semiconductor chip, wherein the dielectric layer is formed to include an opening and a portion of the first electrode surface is exposed through the opening". Applicant respectfully submits that the Examiner cited no portion of Tonti or Kramer that describes or suggests a method including forming a "dielectric layer" as recited in claims 6 and 24. Applicant also notes that claim 24 is also discussed below in connection with the rejection of its dependent claims 27-32.

Applicant also respectfully submits that the Examiner cited no portion of the art that describes or suggests "forming a hole by an anodic forming method" as recited in claim 6.

In addition, the Examiner stated on page 3 of the Office Action that Tonti "does not expressly disclose the hole that is etched through the chip to the opposite surface." The Examiner then cited Kramer, specifically Kramer Fig. 2B and reference numbers 1, 7, and 9. There does not appear to be a Fig. 2B or reference numbers 1, 7 and 9 in Kramer. As a result, it is unclear exactly what portion of Kramer the Examiner is relying on. The Examiner may have intended to cite U.S. Patent No. 5,994,763 to Ohmuro, which was cited in a previous action. Even if the Examiner intended to cite Ohmuro, applicant respectfully submits that neither Ohmuro or Tonti appears to describe or suggest a method including forming a dielectric layer as recited in claims 4 and 24.

The Examiner also cited the abstract of Kramer as mentioning forming stacked integrated circuits. However, the Examiner cited no other portion of Kramer relating to stacked integrated circuits. Applicant notes that Kramer appears to discuss stacking integrated circuits with respect to Figs. 4A and 4B. These figures do not appear to show structures including the formation and positioning of the various layers as recited in the claims, and it is unclear from the Examiner's citations exactly how or why the references would be combined. Thus, the combination of Tonti and Kramer appears to be deficient.

Accordingly, for at least the above reasons, applicant respectfully submits that the rejection of claim 4 and its dependent claim 5, claim 6, and claim 24 and its dependent claims 25-26 and 32, should be withdrawn.

Claims 23 and 27-32 were rejected under 35 U.S.C. 103(a) as unpatentable over Kramer and Tonti, and further in view of U.S. Patent No. 5,805,427 to Hoffman. ("Hoffman"). The rejection is respectfully traversed.

The Examiner cited Hoffman for its disclosure of a insulation layer such as resin, for example, a die attach layer as shown by Hoffman in Fig. 1, including layer 16 and layer 28 attached by die attach layer 30. Applicant notes that Hoffman describes attaching the semiconductor device 28 to the base 14 using the die attach 30 and also using separate bonding wires 32 to electrically interconnect the device 28 to the base 14. As seen in Fig. 1 of Hoffman, the die attach material extends all the way across an upper surface of the semiconductor device 28. The bonding wires 32 on the semiconductor device extend from a lower surface of the device to ends 24 of circuit traces on the base 14. Thus, Hoffman appears to describe connecting the semiconductor device to the base using a die attach material on one surface of the semiconductor device and electrically connecting another surface of the semiconductor device to the base.

The Examiner did not meet his burden to establish a suggestion or motivation in the art for the proposed combination of Kramer, Tonti and Hoffman. According the MPEP section 706.02(j), to establish a prima facie case of obviousness, the following criteria should be met. First, there should be a suggestion or motivation in the art to modify the reference or to combine reference teachings. Second, there should be a reasonable expectation of success. Third, the reference(s) must teach all the claim limitations. MPEP section 706.02(j).

Applicant respectfully submits that the Examiner's citations are insufficient to satisfy the criteria above and accordingly, the rejection should be withdrawn. Applicant respectfully submits that one of ordinary skill in the art would not be motivated to make the combination of references suggested by the Examiner, and the combination does not describe all of the claim limitations. As described above, Hoffman appears to describe using the insulating die attach material to connect the lower structure 28 to the upper structure 14. Tonti appears to describe using a conducting metal material 30 to connect a lower structure 10 with an upper structure 24. To combine Hoffman with Tonti one would at best perhaps replace the metal layer 30 of Tonti with the insulating die attach material and then use separate wiring lines as described in Hoffman to electrically connect the devices. This would appear to teach away from the method of Tonti for making such a connection. Moreover, the Examiner cited no portion of the art suggesting or describing the formation of a "dielectric layer on the interior surface" and an electrical connection through an opening, as recited in claim 23, for example. Specifically, the Examiner's citations to

the art do not describe or suggest "forming a dielectric layer on the interior surface of the first substrate, the dielectric layer having an opening therein, and positioning the dielectric layer so that a portion of the first electrode is exposed through the opening; and positioning the second electrode in the opening and electrically connecting the first electrode to the second electrode through the opening" as recited in claim 23. Absent any such suggestion in the art, the combination of references is deficient and the rejection should be withdrawn.

Claims 27-32 depend from claim 24, which recites in part a method including "forming a dielectric layer on the interior sidewalls of the semiconductor chip, wherein the dielectric layer is formed to include an opening and a portion of the first electrode surface is exposed through the opening; . . . and positioning the second electrode within the hole and in electrical contact with the first electrode." For similar reasons as described above, the Examiner's proposed combination of references is deficient and the rejection should be withdrawn.

Claims 38-39 were rejected under 35 U.S.C. 103(a) as unpatentable over Kramer and further in view of U.S. Patent No. 5,051,811 to Williams et a. ("Williams"). The rejection is respectfully traversed. Claims 38-39 depend from claim 1. The Examiner's citation to Williams does not overcome the deficiencies of Kramer as explained above for claim 1. In addition, the Examiner's citations to Williams do not appear to clearly describe a method including forming a multi-layer electrode including a first conducting layer of tungsten and a second conducting layer of aluminum as recited in claim 39. For at least the reasons described above, applicant respectfully submits that the rejection of claims 38-39 should be withdrawn.

Applicant thanks the Examiner for indicating that claims 34-37 were allowed and that claim 33 would be allowable if rewritten in independent form. Applicant notes that claim 33 was rewritten in independent form in the previous response. Applicant respectfully submits that claim 33 is in allowable form.

The Office Action also included various comments concerning the art and the non-patentability of features in various of the pending claims. Applicants respectfully disagree with the Examiner's combination of the art and non-patentability conclusions. The discussion above has directly addressed some of those comments and the Examiner's other comments are deemed moot at this time in view of this response. For at least the reasons stated above, applicant

respectfully submits that the pending claims are in patentable form. Reexamination and reconsideration are respectfully requested. If, for any reason, the application is not in condition for allowance, the Examiner is requested to telephone the undersigned to discuss the steps necessary to place the application into condition for allowance.

Respectfully submitted,

Alan S. Raynes
Reg. No. 39,809
KONRAD RAYNES & VICTOR, LLP
315 South Beverly Drive, Suite 210
Beverly Hills, CA 90212
Customer No. 24033

Dated: January 23, 2004

(310) 556-7983 (tele general)
(310) 871-8448 (tele direct)
(310) 556-7984 (facsimile)

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on January 23, 2004.

Alan S. Raynes **January 23, 2004**
(Date)